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Please find below and/or attached an Office communication concerning this application or proceeding.

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DETAILED ACTION

1. This Office Action is in response to the remarks filed 5/17/10. Claims 1-20 are currently pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3, 6-10, 13, and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Reches (U.S. Publication US 2002/0110086 A1) in view of Fan (U.S. Pat. 5412648).

With respect to claims 1 and 8, Reches discloses a non-blocking crossbar and method of operation **(See page 2 paragraph 24 of Reches for reference to a crossbar switch and a method for controlling the crossbar switch such that packets are not blocked by each other)**. Reches also discloses n inputs and n outputs **(See page 4 paragraphs 51-52 and Figure 1 of Reches for reference to the switch comprising N input ports and N output ports)**. Reches further discloses each of the outputs having a destination FIFO and n crossbar FIFOs wherein each of the n crossbar FIFOs interposes a corresponding one of each of said n inputs and the

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destination FIFO (**See page 4 paragraph 52, page 4 paragraph 55, and Figure 1 of Reches for reference to each output port having at least one output queue, which is an output FIFO, and for reference to input ports maintaining an output queue for each possible output port, meaning for each output port there are N queues corresponding to each of the N inputs and each of the queues are interposed between a corresponding one of the N inputs and the destination FIFO**). Reches also discloses each of the n interposing crossbar FIFOs being unique to one of the n outputs (**See page 4 paragraph 55 and Figure 1 of Reches for reference to each of the output queues maintained by the input ports storing packets destined to each separate n output port, meaning each of these output queues is unique to a respective one of the n output ports**). Reches also discloses a scheduler configured to cause a plurality of packets that are unencapsulated, unsegmented, and of differing lengths to be transmitted from one of the inputs toward one of the outputs when both the destination FIFO and an interposing one of the crossbar FIFOs have sufficient memory to contain an entirety of a packet of the plurality of packets (**See page 1 paragraph 8, page 4 paragraph 56 to page 5 paragraph 59, and Figure 1 of Reches for reference to forwarding variable length packets that are not segmented or encapsulated and for reference to a scheduler 40 that causes packets to be sent from an input to an output only when it is determined that there is sufficient memory and resources to send the entire packet in a set of time slots where the packet will not be blocked by other packets currently being sent**). Reches does not specifically disclose causing packets to be transmitted only when a destination FIFO

and an interposing one of the crossbar FIFOs have sufficient memory at the same time to receive and then contain an entirety of the packets.

With respect to claims 1 and 8, Fan, in the field of communications, discloses scheduling packets to be transmitted through a switch only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of a packet **(See the abstract, column 3 line 37 to column 4 line 39 and Figure 1 of Fan for reference FIFOs having counters to count the amount of idle space available in the FIFOs and reporting the amount of available space such that packets are sent from an input a destination FIFO only when the FIFOs have a sufficient amount of idle space for accepting an entire cell)**. Scheduling packets to be transmitted through a switch only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of a packet has the advantage of allowing packets to be more smoothly transmitted from an input through all intervening FIFOs to an output to prevent blocking at caused by congestion at any intervening FIFO.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Fan, to combine scheduling packets to be transmitted only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of the packets, as suggested by Fan, with the system and method of Reches, with the motivation being to allow packets to be more smoothly transmitted from an input

through all intervening FIFOs to an output to prevent blocking at caused by congestion at any intervening FIFO.

With respect to claims 2 and 9, Reches discloses that the scheduler is further configured to select one of the inputs based upon a priority thereof **(See page 2 paragraph 18 of Reches for reference to forwarding packets from selected source ports based on priority level of the source port)**.

With respect to claims 3 and 10, Reches discloses that the scheduler is further configured to select one of the outputs based upon a priority thereof **(See page 4 paragraph 52 for reference to scheduler 40 forwarding packets to output ports based on output port queue priority levels)**.

With respect to claims 6 and 13, Reches discloses each output comprising an output arbiter configured to select one of the crossbar FIFOs and transfer a packet therein to the destination FIFO **(See page 4 paragraph 52 and page 5 paragraph 58 for reference to each output port having an arbiter that uses an arbitration scheme to transfer packets from input queues to output queues)**.

With respect to claims 7 and 14, Reches discloses that the arbiter is further configured to select one of the crossbar FIFOs based upon packet priority **(See page 3 paragraph 36 of Reches for reference to selecting packets to be transferred from input queues to output queues based on the priority of the packet)**.

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4. Claims 4, 5, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reches in view of Fan and in further view of Chen et al. (U.S. Pat. 6975638 B1).

With respect to claims 4, 5, 11, and 12, the combination of Reches and Fan does not specifically disclose that at least two of the n inputs are coupled to different types of packet based fabrics with the inputs and outputs being connected to a SONET network and two Ethernet networks.

With respect to claims 4, 5, 11, and 12, Chen et al. discloses a crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network (**See column 5 lines 7-18 and Figure 3 of Chen et al. for reference to a crossbar switching having inputs connected to Gigabit Ethernet networks and a SONET network**). A crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network has the advantage of allowing the switch to transfer packet from both SONET and Ethernet network, which are highly used packet protocol networks.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Chen et al., to combine a crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network, as suggested by Chen et al., with the system and method of Reches and Fan., with the motivation being to allow the switch to transfer packet from both SONET and Ethernet network, which are highly used packet protocol networks.

5. Claims 15-17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reches in view of Fan and in further view of Hartmann et al. (U.S. Pat. 5905873).

With respect to claim 15, Reches discloses a multi-channel network line card for packet based networks **(See page 4 paragraphs 51-52 and Figure 1 of Reches for reference to a switch having input ports that correspond to a line multi-channel network line card)**. Reches also discloses n physical interfaces and inputs numbering at least three **(See page 4 paragraphs 51-52 and Figure 1 of Reches for reference to the switch comprising N input ports, which are physical interfaces, numbering at least three)**. Reches further discloses a non-blocking crossbar coupled to the physical interfaces **(See page 4 paragraphs 51-52 and Figure 1 of Reches for reference to a configurable switch unit 50, which corresponds to a non-blocking crossbar coupled to the input ports)**. Reches also discloses n outputs that transmit the packet to corresponding ones of the n physical interfaces **(See page 4 paragraphs 51-52 and Figure 1 of Reches for reference to the switch comprising N output ports transmitting packets to physical interfaces)**. Reches further discloses each of the outputs having a destination FIFO and n crossbar FIFOs wherein each of the n crossbar FIFOs interposes a corresponding one of each of the n inputs and the destination FIFO **(See page 4 paragraph 52, page 4 paragraph 55, and Figure 1 of Reches for reference to each output port having at least one output queue, which is an output FIFO, and for reference to input ports maintaining an output queue for each possible output port, meaning for each output port there are N queues corresponding to each of the N inputs and each of the queues are interposed**

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between a corresponding one of the N inputs and the destination FIFOs. Reches also discloses each of the n interposing crossbar FIFOs being unique to one of the n outputs **(See page 4 paragraph 55 and Figure 1 of Reches for reference to each of the output queues maintained by the input ports storing packets destined to each separate n output port, meaning each of these output queues is unique to a respective one of the n output ports).** Reches also discloses a scheduler configured to cause a plurality of packets that are unencapsulated, unsegmented, and of differing lengths to be transmitted from one of the inputs toward one of the outputs when both the destination FIFO and an interposing one of the crossbar FIFOs have sufficient memory to contain an entirety of a packet of the plurality of packets **(See page 1 paragraph 8, page 4 paragraph 56 to page 5 paragraph 59, and Figure 1 of Reches for reference to forwarding variable length packets that are not segmented or encapsulated and for reference to a scheduler 40 that causes packets to be sent from an input to an output only when it is determined that there is sufficient memory and resources to send the entire packet in a set of time slots where the packet will not be blocked by other packets currently being sent).** Reches does not specifically disclose causing packets to be transmitted only when a destination FIFO and an interposing one of the crossbar FIFOs have sufficient memory at the same time to receive and then contain an entirety of the packets. Reches also does not specifically disclose n network processors that convert a packet between protocols coupled to corresponding ones of the n physical interfaces.

With respect to claim 15, Fan, in the field of communications, discloses scheduling packets to be transmitted through a switch only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of a packet **(See the abstract, column 3 line 37 to column 4 line 39 and Figure 1 of Fan for reference FIFOs having counters to count the amount of idle space available in the FIFOs and reporting the amount of available space such that packets are sent from an input a destination FIFO only when the FIFOs have a sufficient amount of idle space for accepting an entire cell)**. Scheduling packets to be transmitted through a switch only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of a packet has the advantage of allowing packets to be more smoothly transmitted from an input through all intervening FIFOs to an output to prevent blocking at caused by congestion at any intervening FIFO.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Fan., to combine scheduling packets to be transmitted only when a destination FIFO and an interposing crossbar FIFO have sufficient memory at the same time to receive and then contain an entirety of the packets, as suggested by Fan, with the system and method of Reches, with the motivation being to allow packets to be more smoothly transmitted from an input through all intervening FIFOs to an output to prevent blocking at caused by congestion at any intervening FIFO.

With respect to claim 16, Reches discloses a fast pattern processor that receives a packet from a physical interface and analyzes and classifies the packet **(See page 3 paragraph 36 of Reches for reference to an input port receiving a packet and analyzing the packet to determine parameters including the priority of the packet, which is a classification of the packet)**. Reches does not disclose processing the packet and converting the packet into an appropriate network protocol.

With respect to claims 15 and 16, Hartmann et al., in the field of communications, discloses network processors coupled to corresponding physical interfaces that convert received packets between protocols **(See the abstract of Hartmann et al. for reference to port adaptors, which are network processors, coupled to input ports, which are physical interfaces, that receive packets and convert them between different types of communication formats, which are protocols)**. Using network processors coupled to corresponding physical interfaces that convert received packets between protocols has the advantage of allowing all packets being sent through a crossbar switch to have a common protocol, such that it is easier to switch the packets **(See the abstract of Hartmann et al. for reference to this advantage)**.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Hartmann et al., to combine using network processors coupled to corresponding physical interfaces that convert received packets between protocols, as suggested by Hartmann et al., with the system and method of

Reches and Fan, with the motivation being to allow all packets being sent through a crossbar switch to have a common protocol, such that it is easier to switch the packets.

With respect to claim 17, Reches discloses that the scheduler is further configured to select one of the inputs based upon a priority thereof **(See page 2 paragraph 18 of Reches for reference to forwarding packets from selected source ports based on priority level of the source port)**. Reches also discloses that the scheduler is further configured to select one of the outputs based upon a priority thereof **(See page 4 paragraph 52 for reference to scheduler 40 forwarding packets to output ports based on output port queue priority levels)**.

With respect to claim 20, Reches discloses each output comprising an output arbiter configured to select one of the crossbar FIFOs and transfer a packet therein to the destination FIFO **(See page 4 paragraph 52 and page 5 paragraph 58 for reference to each output port having an arbiter that uses an arbitration scheme to transfer packets from input queues to output queues)**. Reches discloses that the arbiter is further configured to select one of the crossbar FIFOs based upon packet priority **(See page 3 paragraph 36 of Reches for reference to selecting packets to be transferred from input queues to output queues based on the priority of the packet)**.

6. Claims 18 and 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Reches in view of Fan and Hartmann et al. and in further view of Chen et al.

With respect to claims 18 and 19, the combination of Reches, Fan, and Hartmann et al. does not specifically disclose that at least two of the n inputs are coupled to different types of packet based networks with the inputs and outputs being connected to a SONET network and two Ethernet networks.

With respect to claims 18 and 19, Chen et al. discloses a crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network (**See column 5 lines 7-18 and Figure 3 of Chen et al. for reference to a crossbar switching having inputs connected to Gigabit Ethernet networks and a SONET network**). A crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network has the advantage of allowing the switch to transfer packet from both SONET and Ethernet network, which are highly used packet protocol networks.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Chen et al., to combine a crossbar switch with inputs connected to Gigabit Ethernet networks and a SONET network, as suggested by Chen et al., with the system and method of Reches, Fan, and Hartmann et al., with the motivation being to allow the switch to transfer packet from both SONET and Ethernet network, which are highly used packet protocol networks.

Response to Arguments

7. Applicant's arguments filed 5/17/10 have been fully considered but they are not persuasive.

Regarding Applicant's argument that Reches does not disclose the current claim limitation stating "wherein each of said n crossbar FIFOs interposes a corresponding one of each of said n inputs". First, the examiner agrees with the Applicant's argument that the specification does not disclose the suggested limitation of "wherein each of said n crossbar FIFOs interposes every input and said destination FIFO", thus the Examiner's suggestion to change the claim language is withdrawn. In light of this argument, it is believed that Reches does disclose the current claim limitation and an equivalent configuration as shown in Applicant's Figure 2. Figure 2 of the specification discloses n inputs (with $n=3$), n outputs, and n crossbar FIFOs of each the n outputs with each of the n crossbar FIFOs interposing a corresponding one of each of said n inputs and a destination FIFO. For example, Figure 2 shows output 1 including CB FIFOs 210, 212, and 214, wherein CB FIFO 210 interposes input 1 and destination FIFO 216, wherein CB FIFO 212 interposes input 2 and destination FIFO 216, and wherein CB FIFO 214 interposes input 3 and destination FIFO 216. Reches discloses an equivalent configuration to that of Applicant's Figure 2. Reches discloses a switch having n inputs, n outputs, and n crossbar FIFOs of each the n outputs with each of the n crossbar FIFOs interposing a corresponding one of each of said n inputs and a destination FIFO (See page 4 paragraph 52, page 4 paragraph 55, and Figure 1 of Reches for reference to a switch having n inputs, n outputs, and n queues Q , which are crossbar FIFOs, of each of the n outputs with each of the n queues Q interposing a corresponding one of each of the n inputs and an output queue). The queues Q of Reches are each indexed by an ordered pair $Q(x,y)$ wherein x refers to an input

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corresponding to the queue and y refers to an output corresponding to the queue.

Thus, for example, Figure 2 of Reches shows output 1 that has queues $Q(1,1)$,...

$Q(M,1)$,... and $Q(N,1)$, wherein $Q(1,1)$ interposes input 1 and the output queue of output

1, wherein $Q(M,1)$ interposes input M and the output queue of output 1, and wherein

$Q(N,1)$ interposes input N and the output queue of output 1. The table below is used to

provide a further comparison between the claim language, Figure 2 of the Applicant's specification, and Figure 1 of Reches.

<u>CLAIM LANGUAGE</u>	<u>APPLICANT'S FIGURE 2</u>	<u>RECHES FIGURE 1</u>
n inputs	input 1, input 2, and input 3; wherein $n=3$	inputs 1-N
n outputs	output 1, output 2, and output 3; wherein $n=3$	outputs 1-N
each output having a destination FIFO	destination FIFO 216 of output 1, destination FIFO 226 of output 2, and destination FIFO 236 of output 3	each output having an output queue (See page 4 paragraph 52)
n crossbar FIFOs interposing a corresponding one of each of the n inputs and said destination FIFO	crossbar FIFOs 210, 212, and 214 respectively between corresponding inputs 1, 2, and 3, and destination FIFO 216	Queues $Q(1,1)$, $Q(M,1)$, and $Q(N,1)$ respectively between corresponding inputs 1, M, and N and the output queue of output 1

Therefore, Reches does disclose the current claim limitation stating “wherein each of said n crossbar FIFOs interposes a corresponding one of each of said n inputs” and also discloses an equivalent configuration to that of the Applicant’s Figure 2.

Regarding Applicant’s argument that Ku et al. teaches away from using an additional destination FIFO, the Examiner respectfully disagrees. Applicant argues that the process of selection of packets from buffers disclosed by Ku et al. prohibits the use of a destination FIFO. It is unclear why packets selected from different buffers of Ku et al. could not be then stored in an output buffer. Since each output port can only output one packet at a time adding a destination output FIFO between the buffers and the output allows multiple packets to be selected in order for output in advance such that the output port does not have to wait for packets to be selected.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON E. MATTIS whose telephone number is (571)272-3154. The examiner can normally be reached on M-F 8AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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